

REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the outstanding Office Action, the specification is objected to because it allegedly provides insufficient antecedent basis for the claimed limitation that "said gate comprising Re contains no halogens therein". Although applicants believe that the originally filed specification provides adequate support for the claim limitation previously added to Claims 1 and 10, applicants have nevertheless cancelled the aforementioned phrase from each of Claims 1 and 10.

In view of the above amendment to Claims 1 and 10, the objection to the specification can and should be withdrawn.

In addition to the foregoing amendment to Claims 1 and 10, applicants have also amended those claims to positively recite that *the gate comprising Re has an interface trapped charge density of about $3E 10 \text{ cm}^{-2} \text{ eV}^{-1}$ to about $4E 10 \text{ cm}^{-2} \text{ eV}^{-1}$* . Support for this claim amendment to Claims 1 and 10 is found in paragraph [0057] and [0061] of the original U.S. Patent Application publication No. 2003/0098489 A1. Since the above amendment to Claims 1 and 10 does not introduce new matter into the specification of the instant application, entry thereof is respectfully requested.

Claims 1, 2, 5, 7-11 and 14-16 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over U.S. Patent No. 6,300,208 to Talwar et al. ("Talwar et al."). Claims 1, 2, 4, 7-11 and 13-16 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of U.S. Patent Application Publication No. 2001/0032995 to Maria et al. ("Maria et al.") and Talwar et al.

Applicants respectfully submit that Talwar et al., alone, or Maria et al. in combination with Talwar et al. do not render the claimed structures obvious. Specifically, Talwar et al., alone, or the combination of Maria et al. and Talwar et al., do not teach or suggest a structure including a Re gate electrode wherein the Re gate electrode has *an interface trapped charge density of about $3E 10\text{ cm}^{-2}\text{ eV}^{-1}$ to about $4E 10\text{ cm}^{-2}\text{ eV}^{-1}$* , as presently claimed. Applicants observe that in the present application (see paragraphs [0057] and [0061]) the now claimed interface charge density for the Re gate is obtained by utilizing a passivation anneal that is performed at a high H_2 pressure (about 400 torr) and at 350°C . As indicated in the originally filed specification, the now claimed range of interface trapped charge densities is reduced from that achieved utilizing a conventional forming gas anneal.

Talwar et al. disclose Re gate electrodes that are formed via many different techniques. CVD, PVP and PECVD are specific deposition processes mentioned in Talwar et al. that can be used in forming the Re gate electrode. Talwar et al. do not teach or suggest any passivation step, let alone one that provides their disclosed Re gates with the now claimed interface trapped charge density range. As such, the claims of the present application are not rendered obvious from the disclosure of Talwar et al.

With respect to the combination of Maria et al. and Talwar et al., applicants submit that Maria et al. are defective in that it does not teach or suggest the use of a Re gate electrode, let alone the claimed Re gate electrode has *an interface trapped charge density of about $3E 10\text{ cm}^{-2}\text{ eV}^{-1}$ to about $4E 10\text{ cm}^{-2}\text{ eV}^{-1}$* . Applicants observe that in Maria et al. the Pt gate electrode can be passivated by annealing at 350°C in 5% hydrogen, the balance being Ar. Applicants submit that the annealing disclosed in Maria et al. is not a forming gas annealing; a forming gas includes H_2

and N₂). As such, Maria, et al. do not teach or suggest an annealing technique that is capable of providing the claimed range of interface trapped charge densities within a Re gate.

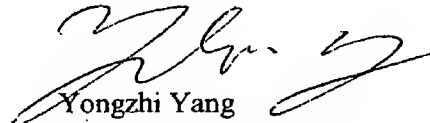
This aforementioned defect in Maria et al. is not obviated by the disclosure of Talwar et al. since the applied secondary reference also does not teach or suggest a Re gate electrode that contains no halogen, as presently claimed. Applicants again observe that Talwar et al. disclose Re gate electrodes that are formed via many different techniques. CVD, PVP and PECVD are specific deposition processes that can be used in forming the Re gate electrode. Although Talwar et al. mention that the Re gate can be formed by CVD, the applied reference fails to disclose a *Re gate having an interface trapped charge density of about $3E 10\text{ cm}^{-2}\text{ eV}^{-1}$ to about $4E 10\text{ cm}^{-2}\text{ eV}^{-1}$* . As such, the claims of the present application are not rendered obvious from the combined disclosures of Maria et al. and Talwar et al.

The various § 103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed structures to include the various elements, particularly the that the Re gate *has an interface trapped charge density of about $3E 10\text{ cm}^{-2}\text{ eV}^{-1}$ to about $4E 10\text{ cm}^{-2}\text{ eV}^{-1}$* , as presently recited in the claims of the present application. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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